IN THE ABSTRACT

Please replace the Abstract beginning on page 48, line 7, with the following rewritten Abstract:

A Storage Reference Buffer (SRB) designed as an autonomous unit for all Store operations that transfer data from the execution unit of a processor to the memory hierarchy and Load operations that transfer [[of]] data from the memory hierarchy to the execution unit of the processor. The SRB partitions up the Load and Store operations into several smaller operations in order to perform them in parallel with other Load and Store requests. System elements are included to determine unambiguously which of these Load and Store operations may be performed without waiting for prior operations to be completed. The SRB also includes system elements to detect whether requests may be satisfied by existing entries in the SRB without having to access the cache. The SRB is operated as a content addressable memory. Load request are simultaneously launched to cache and to the SRB with the Cache request being canceled if the Load request may be satisfied by an SRB entry.